LELO_GR04_SKY130A

Table of Contents

- Who
- Why
- How
  - Bandgap circuit
    - Mini Theory
    - Design Parameters and Values
    - MOSFET Configurations & Sizing
    - Result
  - Oscillator
    - Theory
    - Implementation
    - Result
  - Digital counter
    - Theory
    - Testbench
  - Layout
    - Analog
    - Digital
    - TinyTapeout block
- What
- Signal interface
- Key parameters

Who

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Why

To generate a **PTAT (Proportional To Absolute Temperature)** current and a **CTAT (Complementary To Absolute Temperature)** voltage, we use a bandgap reference circuit.

How

Bandgap circuit

Mini Theory: The design is according to Milestone 1 of the project:

The two diodes carry the same current I_D, forced by the operational amplifier, so:

$$\Delta V_D = V_{D1} - V_{D2} = V_T \ln\left(\frac{I_D}{I_{S1}}\right) - V_T \ln\left(\frac{I_D}{I_{S2}}\right) = V_T \ln\left(\frac{I_{S2}}{I_{S1}}\right) \Rightarrow \Delta V_D = V_T ln(N)$$

which is **PTAT**. N is the current density ratio between the two diodes, and if they have the same current, then N is also the effective area ratio of the p-n junctions.

The op-amp forces the top node voltages equal, giving:

$$V_{D1} = V_{D2} + IR_1 \Rightarrow I = \frac{\Delta V_D}{R_1} = \frac{kT}{qR_1}\ln(N)$$

Therefore the circuit generates a PTAT current.

If we want to create a bandgap reference, mirroring this current into a branch with R_2 and diode D_3 gives:

$$V_{\text{REF}} = V_{D3} + IR_2 = V_{D3} + \frac{R_2}{R_1}\Delta V_D$$

Since V_{D3} is **CTAT** and ΔV_D is **PTAT**, choosing the ratio $\frac{R_2}{R_1}$ such that $\frac{dV_{\text{REF}}}{dT} = 0$ allows us to cancel the temperature dependence.

Since we want a **temperature sensor** instead of a stable reference, we measure the I_{PTAT} directly.
Design Parameters and Values:

Parameter	Specification / Target	Notes
Diode Resistor (R_{diode})	$\approx$ 30 kΩ	Using RPPO4
p-n junction ratio	8	Diode-connected BJTs
IPTAT @ 25C	$\approx 1.78\mu A$	
Input MOSFET Pair	5F0	Differential pair
Tail Resistor (R_{tail})	RPPO2	
Bias Current (I_D)	1.8μA $\rightarrow$ 7μA	Target: $\approx 5\mu$A
Settling time constant (τ)	0.2μs	$\tau = R_{\text{out}}C_C$
Compensation (C_C)	$\approx$ 0.1 pF	Given $R_{\text{out}} \approx$ 2 MΩ

MOSFET Configurations & Sizing: **Input Pair & Tail Resistor**

The BJT used is the default PNP in the JNW_TR_SKY130A library. A 1:8 ratio was chosen to ease layout and gradient effects later. V_{be} is roughly 0.7-0.85 V at room temp, and this is the common mode input voltage. Based on this a PMOS input pair was chosen.

The available transistors are in the JNW_ATR_SKY130A library. We want the following criteria:

- **Low mismatch**: requiring larger transistors (5F0 and preferably wide transistors).
- **gm/id = 15**: with 10, the V_{sg} of 5F0 transistors are too high for the tail resistor.
- **Rtail** $\in$ **[15k, 120k]**: the JNW_TR_SKY130A provides this range of resistors (RPPO2 -> RPPO16), and we do not want to exceed them to save area.

- **Cc ∈ [50nF, 500nF]**: the JNW_TR_SKY130A provides 50nF (X1) and 200nF (X4) capacitors. The settling time of the bandgap circuit should be ~ 1us to give time for the rest of circuit. This means $\tau = r_{out}C_c \approx 0.2us$.

Based on the available components, we select $I_{bias} \approx 5\mu A$ and RPPO2 resistor (15k Ω). This gives ~ 150 mV voltage drop across the resistor, but this will change a lot depending on V_{icm}.

To pass $5\mu A$ current at $g_m/I_D = 15$:

- **Option A:** $5 \times 8C\ 5F0$
- **Option B:** $4 \times 12C\ 5F0$

We finally selected $4 \times 8C\ 5F0$, resulting in slightly lower current for power and area optimization.

Differential Pair Active Load We want the NMOS pair to pass $5\mu A$ each, but we do not want them in too weak inversion. More importantly, we also want output resistances to be on the order of the PMOS input pair. $4 \times 8C\ 5F0$ PMOS in weak inversion has roughly $10M\Omega$ output resistance.

Choosing compensation capacitance $C_c = 0.1pF$, $r_{out} = \tau/C_c \approx 2M\Omega$.

From these two points, we select $2C\ 5F0$ NMOS transistors as active load pair.

Current Mirror For BJT Pair

We want good matching between them and relatively high output resistance -> use 5F0 devices.

Using the **5F0** device with ≈ 2μA bias: * **Configuration:** $4C\ 5F0$ * **Operating Window:** 0.5μA → 3.19μA for g_m/I_D values between 15 → 10.

Start Up Circuit

We first tried Razavi's simple timing circuit to initially keep node `Vp` low. We use a NMOS, which draws current from `Vp` untill VDD stabilizes.

However, this led to large leakage current for some reason. So instead, we directly couple `Vp` to the drain of the gating transistor of the bandgap.

Stability

Since we first have a very low Phase Margin (~ 25°), we use the dominant pole compensation method to increase it.

When PM = 55°: f_t = 22MHz, loop gain = 7.5dB = 2.37.

Therefore Cc >= 2.37 times X1, so we replace X1 with X4. This pushed the PM to 60°. Of course, there is a trade-off between the covering area and the phase margin. We can also add a resistor for lead compensation later.

Regulated Cascode

Following the example in Razavi's, we added a regulated cascode at the PMOS mirror outputs. However, simulation shows that the drain voltages of the PTAT PMOSes are too low, so `VCASCP` simply goes directly to GND.
Result: The simulated IPTAT is not so linear, but may work well enough in the 0°-100°C range. The VCTAT is slightly better, so perhaps a better output mirror structure could improve this IPTAT.

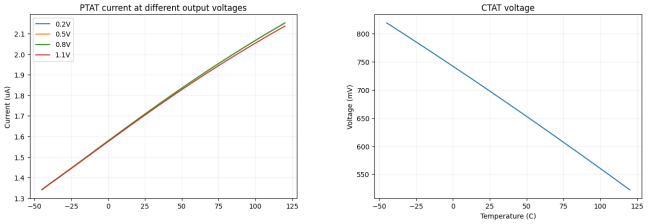


Fig. 1. IPTAT and VCTAT

Oscillator

Theory: The oscillator is based on Milestone 2:

where the capacitor is charged by a PTAT current up to a CTAT voltage, both of which are supplied by the bandgap. The inverters provide a slight delay for the comparator to fully discharge the capacitor, restarting the cycle.

The change of voltage of the capacitor is given by:

$$\frac{dV_C}{dt} = \frac{I_{ptat}}{C}$$

Given constant I_{ptat}, the charging duration is:

$$T_{charge} = V_{ctat} \times C/I_{ptat}$$

If assuming the discharge is instantaneous, the oscillation frequency is:

$$f_{osc} = I_{ptat}/(CV_{ctat})$$

Choosing the capacitor to be 4x CAPX4, each composed of 4 CAPX1 that are 53.8 fF each, and using the following values for I_{ptat} and V_{ctat} (from typical bandgap simulation):

Quantity	Value
`IPTAT @ 25C`	1.693 uA
`IPTAT temperature coefficient`	4.958 nA/K
`VCTAT @ 25C`	708.725 mV
`VCTAT temperature coefficient`	-1.786 mV/K

We arrive at the following expected oscillation frequencies at different temperatures:

Temperature	Expected frequency
-45 C	1.875 MHz
25 C	2.775 MHz
125 C	4.797 MHz

The actual oscillation frequencies can change, depending on layout parasitics and process corners.

Implementation: The oscillator currently uses a second comparator to compare capacitor voltage with half the V_{ctat} voltage, since the D flip-flop is not tested yet. It can be implemented later to reduce current usage. 6 inverters are used to delay the comparator output.
Result: The following are the plots of capacitor voltage, comparator output, and oscillator output at different temperature corners. Process and voltage are typical.

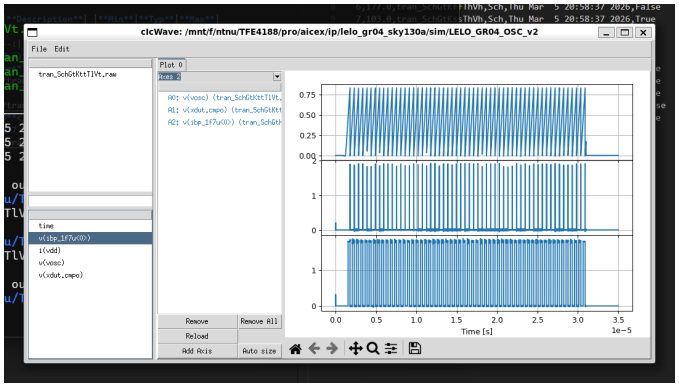


Fig. 2. Oscillator_Tl

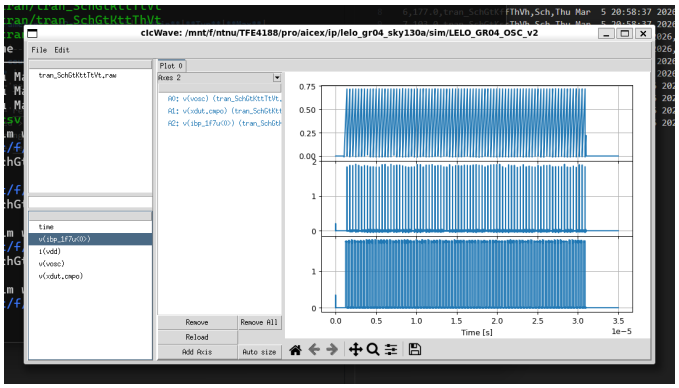


Fig. 3. Oscillator_Tt

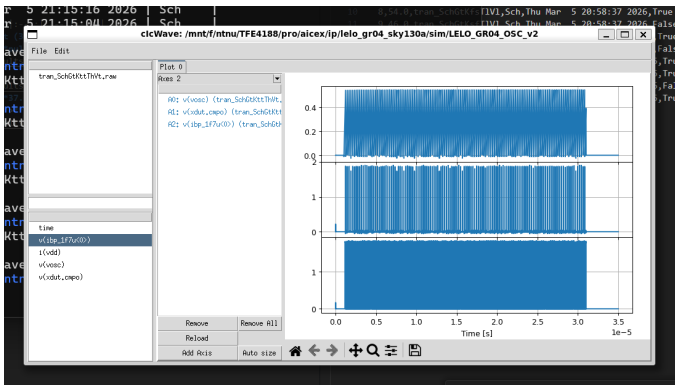


Fig. 4. Oscillator_Th

The plot of oscillation frequency vs. temperature at typical process and voltage is below. The scaled curve is the expected curve scaled (calibrated) to the measurement at 25C. The temperature error predicted by this curve is in the second plot.

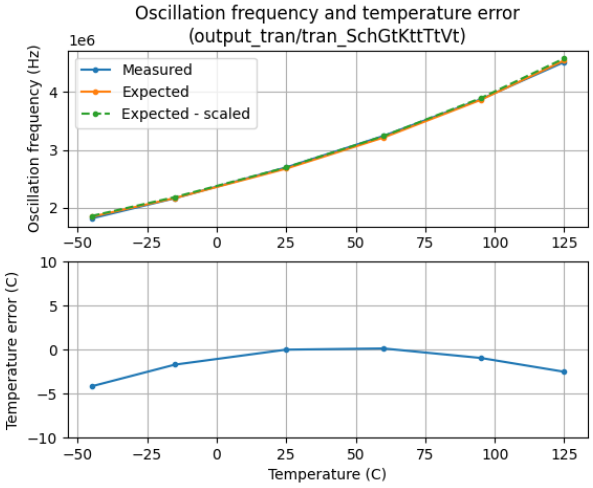


Fig. 5. Count typical

Plots of other corners can be found in the same folder. The majority of them deviate from the expected curve, but the calbiration helps address this. Likely sources of errors are the non-zero delay of the comparator, and the transient startup of the bandgap.

Digital counter

Theory: The digital counter is simple and implemented as the state machine shown below. The reset is asynchronous and active low. When a `start` signal is received, the analog part is enabled via `pwrupOsc` for one 32kHz cycle. In this time, `osc_counter[8:0]` is incremented using the `OSC_TEMP_1V8` signal from analog. 9 bits are used here to accommodate a maximum oscillation frequency of ~16MHz. After the 32kHz finishes, the 8 MSBs are sent to output (`count_value[7:0]`).

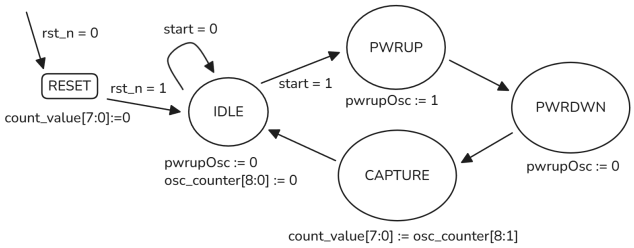


Fig. 6. FSM

From simulations, the actual frequency of the oscillator can reach up to 8MHz due to variations.
Testbench: To test the digital, a 10MHz clock (`osc_clk`) is generated parallel to the 32kHz clock (`clk`). The counter should record ~312 cycles, which is what we see on the `osc_measure[8:0]` signal (`0x138 - 0x139`). It's binary representation is `1_0011_1000`, and the 8 MSBs are `1001_1100` (`0x9C`). This is the output at `count_value[7:0]`. A reset is done mid-simulation to show its functionality.

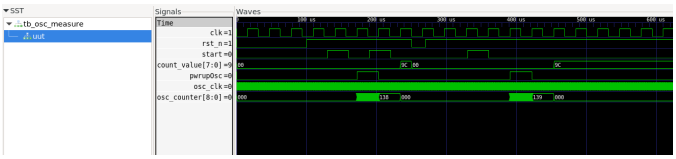


Fig. 7. Testbench

Layout

Analog: The circuit is analog-on-top, so the analog components are placed before the digital block is set in place. The two main components are shown below:

- *Bandgap*: The diode-connected PNP BJTs are on the left, with D_1 in the middle and D_2 around (8 BJTs). This is to cancel out first-order gradient effects on the bandgap operation. On the right, we have the op-amp with tail resistor, and the middle components are the rest of the bandgap. The compensation capacitors can also be seen. Some dummy transistors are added at top and bottom of the bandgap current mirror.

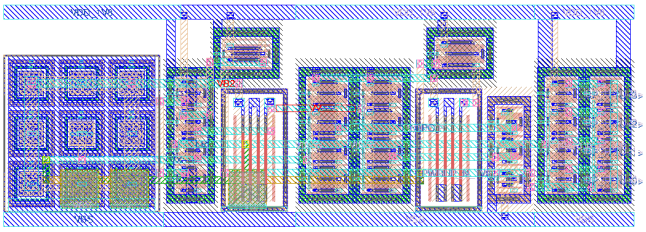


Fig. 8. Bandgap layout

- *Oscillator*: The two comparators are to the left and right of the layout. The middle part is the chain of 6 inverters, as well as the capacitor reset transistors. The large 4x4 capacitor array is the oscillator capacitor, while the 2 capacitors towards the right are the voltage divider.

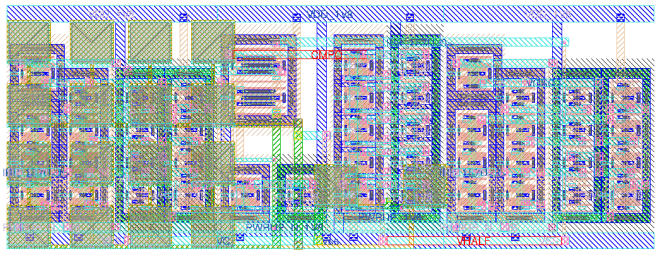


Fig. 9. Bandgap layout

Components on the same layout row share the 2um local-interconnect power rails. The routing metals are a bit thick (1um) to match the S/D metals of the unit transistors. Antenna effect may be a problem with the long routing, so they may change in the future.

Digital: The digital layout is generated by the Librelane classic flow, using the default Google Colab notebook. The resulting notebook, as well as other generated files, is stored in ./rtl. The pin list and other configurations are set up near the beginning of the notebook.

The resulting layout is shown below. The `count_value[7:0]` output pins are placed at the top to go to TinyTapeout's bidirectional outputs, while other signals are routed to the side to interface with analog.

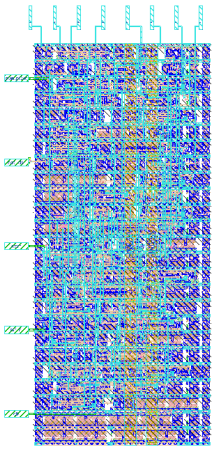


Fig. 10. Digital layout

TinyTapeout block: The combined analog + digital block is shown below. The double power rings are redundant and can change. Currently, the `pwrupOsc` signal is generated by the digital block and routed to output, but an OR gate can be added to also power on the analog block from the outside. A tie-high (on top right) is used to pull up `uio_oe[7:0]` (output enable) pins.

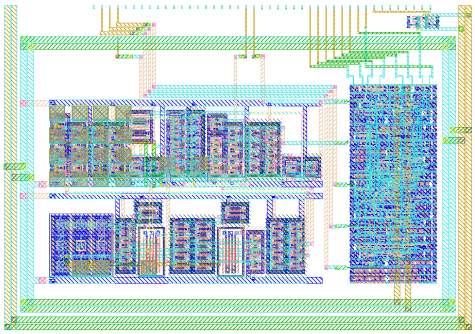


Fig. 11. TT layout

WHAT

What	Cell/Name
Schematic	design/LELO_GR04_SKY130A/LELO_GR04.sch
Layout	design/LELO_GR04_SKY130A/LELO_GR04.mag

SIGNAL INTERFACE

Signal	Direction	Domain	Description
VDD_1V8	Input	VDD_1V8	Main supply
OSC_-TEMP_1V8	Output	VDD_1V8	Temperature dependent oscillation frequency
PWRUP_-1V8	Input	VDD_1V8	Power up the circuit
VSS	Input	Ground	

Key parameters

Parameter	Min	Typ	Max	Unit
Technology		Skywater 130 nm		
AVDD	1.7	1.8	1.9	V
Temperature	-40	27	125	C

Install

Clone LELO_GR04_SKY130A

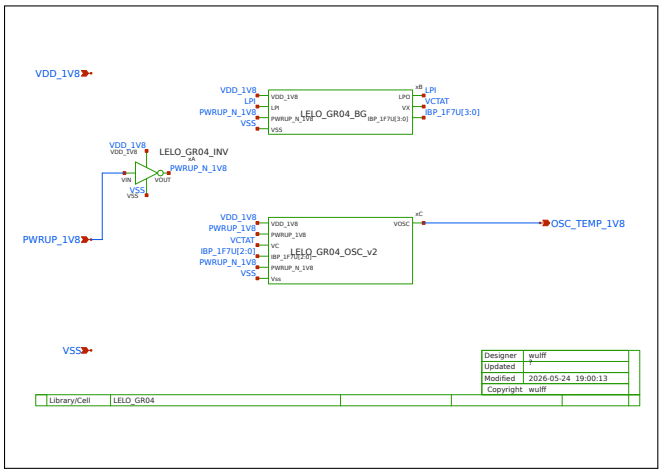
To install, do the following

```
python3 -m pip install cicconf
git clone --recursive https://github.com/analogicus/lelo_gr04_sky130a lelo_gr04_sky130a
cicconf --rundir ./ --config lelo_gr04_sky130a/config.yaml clone --https
```

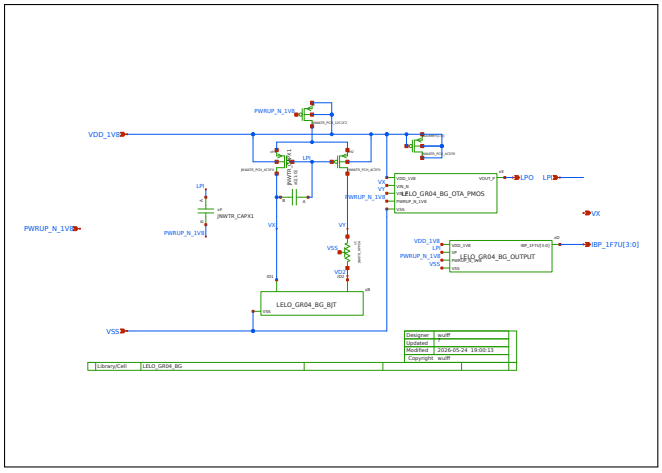
Schematics

LELO_GR04_SKY130A

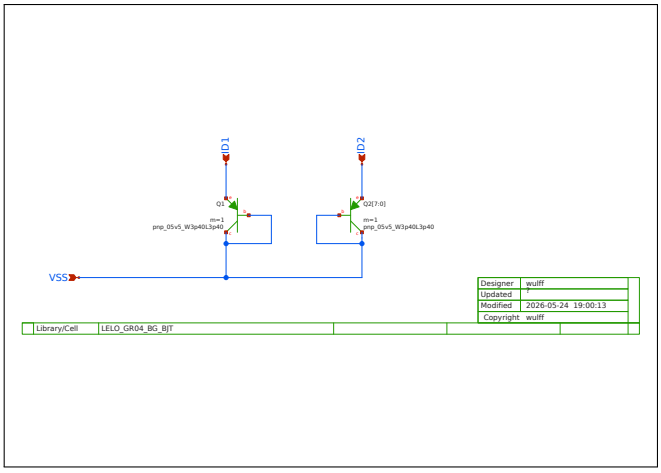
LELO_GR04:



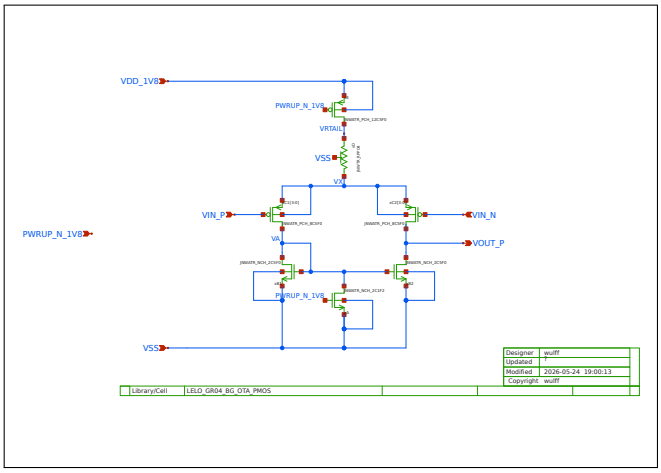
LELO_GR04_BG:



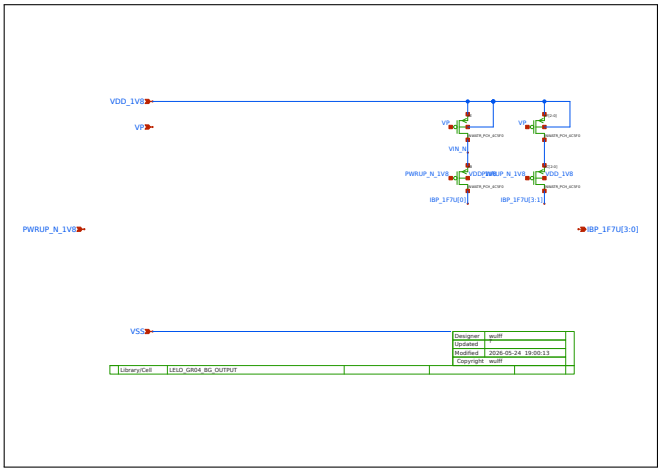
LELO_GR04_BG_BJT:



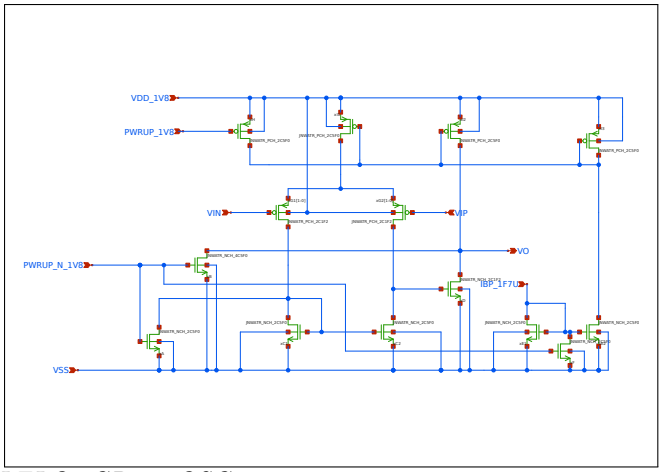
LELO_GR04_BG_OTA_PMOS:



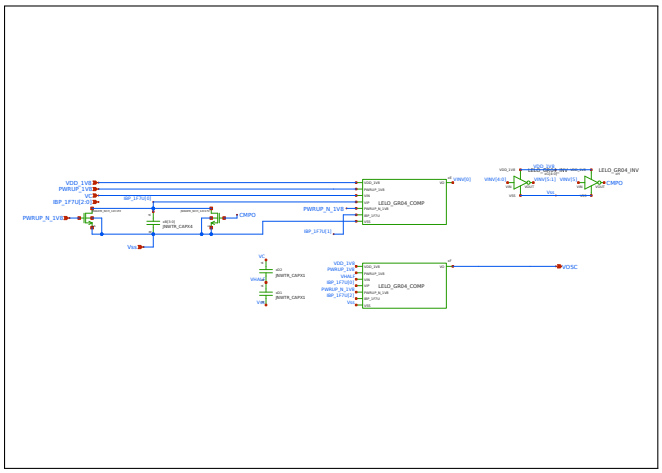
LELO_GR04_BG_OUTPUT:



LELO_GR04_COMP:



LELO_GR04_OSC_v2:



Simulations

LELO_GR04_SKY130A

LELO_GR04: README.md: “8e12614 Tue Apr 28 20:43:27 2026 +0200”

TB_NCM

Transient analysis (tran): Check transient operation

Name	Parameter	Description		Min	Typ	Max	Unit
Active current	**idd__-45**		**Spec**	**10.000**	**40.000**	**70.000**	**uA**
			Sch__typ		14.550		
			Sch__etc__-notemp	**9.061**	14.447	19.170	
			Sch__3std	**8.358**	14.952	21.546	
			Lay__typ		14.579		
			Lay__etc__-notemp	**8.260**	14.487	19.554	
			Lay__3std	**6.921**	14.355	21.789	
Active current	**idd__25**		**Spec**	**10.000**	**40.000**	**70.000**	**uA**
			Sch__typ		23.083		
			Sch__etc__-notemp	17.652	23.163	30.716	
			Sch__3std	17.553	23.322	29.092	
			Lay__typ		23.460		
			Lay__etc__-notemp	17.834	23.538	31.436	
			Lay__3std	16.698	23.255	29.812	
Active current	**idd__125**		**Spec**	**10.000**	**40.000**	**70.000**	**uA**
			Sch__typ		36.946		
			Sch__etc__-notemp	29.076	37.016	47.541	
			Sch__3std	31.487	37.137	42.787	
			Lay__typ		37.853		
			Lay__etc__-notemp	29.602	37.909	49.014	
			Lay__3std	31.108	37.686	44.264	
Leakage current	**iddq__-45**		**Spec**	**0.000**	**50.000**	**100.000**	**nA**
			Sch__typ		1.314		
			Sch__etc__-notemp	0.855	1.150	1.456	
			Sch__3std	0.800	1.197	1.594	
			Lay__typ		1.743		
			Lay__etc__-notemp	1.859	2.622	2.808	
			Lay__3std	1.464	2.490	3.516	
Leakage current	**iddq__25**		**Spec**	**0.000**	**50.000**	**100.000**	**nA**
			Sch__typ		1.913		
			Sch__etc__-notemp	1.256	1.921	8.685	
			Sch__3std	1.454	1.881	2.308	
			Lay__typ		3.424		
			Lay__etc__-notemp	2.720	3.402	11.257	
			Lay__3std	2.577	3.297	4.017	
Leakage current	**iddq__125**		**Spec**	**0.000**	**50.000**	**100.000**	**nA**
			Sch__typ		10.349		
			Sch__etc__-notemp	9.787	15.645	39.508	
			Sch__3std	10.124	10.457	10.790	
			Lay__typ		15.454		
			Lay__etc__-notemp	12.109	20.570	44.940	
			Lay__3std	14.511	15.328	16.145	
Oscillation frequency @ -45C	**fosc__-45**		**Spec**	**1.406**	**1.875**	**2.344**	**MHz**
			Sch__typ		1.813		
			Sch__etc__-notemp	**1.106**	1.797	**2.448**	
			Sch__3std	**0.915**	1.844	**2.774**	
			Lay__typ		1.470		
			Lay__etc__-notemp	**0.850**	1.449	1.943	
			Lay__3std	**0.702**	1.440	2.179	
Oscillation frequency @ 25C	**fosc__25**		**Spec**	**2.081**	**2.775**	**3.469**	**MHz**
			Sch__typ		2.696		
			Sch__etc__-notemp	**2.064**	2.699	**3.644**	
			Sch__3std	**1.773**	2.711	**3.650**	
			Lay__typ		2.168		
			Lay__etc__-notemp	**1.690**	2.170	2.852	
			Lay__3std	**1.427**	2.139	2.852	
Oscillation frequency @ 125C	**fosc__125**		**Spec**	**3.598**	**4.797**	**5.996**	**MHz**
			Sch__typ		4.522		
			Sch__etc__-notemp	**3.470**	4.562	**6.186**	
			Sch__3std	**3.392**	4.527	5.663	
			Lay__typ		**3.550**		
			Lay__etc__-notemp	**2.788**	**3.552**	4.648	
			Lay__3std	**2.616**	**3.517**	4.418	
Temperature error (calibrated @ 25C)	**t__err__max**		**Spec**	**-10.00**	**0.00**	**10.00**	**C**

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TB_NCM

Transient analysis (tran): Check transient operation

Name	Parameter	Description		Min	Typ	Max	Unit
Active current	**idd**		**Spec**	**5.000**	**15.000**	**50.000**	**uA**
			Sch_typ		15.981		
			Sch_etc	7.954	17.419	35.457	
			Sch_3std	11.942	16.140	20.338	
			Lay_typ		17.164		
			Lay_etc	8.496	17.687	35.170	
			Lay_3std	12.373	17.135	21.897	
Leakage current	**iddq**		**Spec**	**0.000**	**0.500**	**1.000**	**nA**
			Sch_typ		**2.032**		
			Sch_etc	0.526	**2.511**	**13.787**	
			Sch_3std	**2.001**	**2.032**	**2.063**	
			Lay_typ		**2.321**		
			Lay_etc	0.720	**3.123**	**13.024**	
			Lay_3std	**2.297**	**2.322**	**2.346**	
Output current @ 0.2-1.1V	**i0**		**Spec**	**1.000**	**1.700**	**2.600**	**uA**
			Sch_typ		2.282		
			Sch_etc	1.520	2.337	**3.463**	
			Sch_3std	1.376	2.311	**3.247**	
			Lay_typ		2.282		
			Lay_etc	1.520	2.337	**3.463**	
			Lay_3std	1.267	2.285	**3.303**	
Output current @ 0.2-1.1V	**i1**		**Spec**	**1.000**	**1.700**	**2.600**	**uA**
			Sch_typ		2.282		
			Sch_etc	1.520	2.337	**3.463**	
			Sch_3std	1.460	2.293	**3.125**	
			Lay_typ		2.282		
			Lay_etc	1.520	2.337	**3.463**	
			Lay_3std	1.260	2.284	**3.308**	
Output current @ 0.2-1.1V	**i2**		**Spec**	**1.000**	**1.700**	**2.600**	**uA**
			Sch_typ		2.282		
			Sch_etc	1.520	2.337	**3.463**	
			Sch_3std	1.395	2.322	**3.248**	
			Lay_typ		2.282		
			Lay_etc	1.520	2.337	**3.463**	
			Lay_3std	1.292	2.268	**3.245**	
Output current @ 0.2-1.1V	**i3**		**Spec**	**1.000**	**1.700**	**2.600**	**uA**
			Sch_typ		2.281		
			Sch_etc	1.520	2.335	**3.448**	
			Sch_3std	1.386	2.311	**3.236**	
			Lay_typ		2.281		
			Lay_etc	1.520	2.335	**3.448**	
			Lay_3std	1.273	2.268	**3.263**	
Bandgap resistor voltage	**vrd**		**Spec**	**30.000**	**52.000**	**80.000**	**mV**
			Sch_typ		54.843		
			Sch_etc	41.248	57.774	75.444	
			Sch_3std	41.090	55.216	69.342	
			Lay_typ		54.843		
			Lay_etc	40.473	57.774	75.444	
			Lay_3std	37.684	54.609	71.534	
Settling time (2%) @ 0.5V	**t_settle_98**		**Spec**	**0.000**	**1.000**	**5.000**	**us**
			Sch_typ		0.078		
			Sch_etc	0.056	0.070	**7.376**	
			Sch_3std	0.073	0.078	0.083	
			Lay_typ		0.106		
			Lay_etc	0.068	0.106	**7.914**	
			Lay_3std	0.088	0.107	0.125	

Loop stability analysis (lstb): Check loop stability of OTA-bandgap

Name	Parameter	Description		Min	Typ	Max	Unit
Gain margin	**gm__db**		**Spec**	**-50.000**	**-20.000**	**-10.000**	**dB**
			Sch__typ		-18.961		
			Sch__etc	-32.718	-18.900	-17.499	
			Sch__3std	-19.149	-18.964	-18.779	
			Lay__typ		-18.325		
			Lay__etc	-29.831	-18.302	-17.763	
			Lay__3std	-18.402	-18.325	-18.248	
Phase margin	**pm__deg**		**Spec**	**45.000**	**60.000**	**90.000**	**deg**
			Sch__typ		86.682		
			Sch__etc	62.961	84.667	89.233	
			Sch__3std	80.092	86.869	**93.646**	
			Lay__typ		83.319		
			Lay__etc	68.218	82.619	87.829	
			Lay__3std	76.962	83.634	**90.306**	
Loop gain	**lf__gain**		**Spec**	**20.000**	**35.000**	**50.000**	**dB**
			Sch__typ		33.867		
			Sch__etc	28.833	32.636	35.187	
			Sch__3std	32.284	33.843	35.403	
			Lay__typ		33.698		
			Lay__etc	28.453	32.664	35.008	
			Lay__3std	32.016	33.611	35.205	
Unity-gain frequency	**f__ug**		**Spec**	**5.000**	**15.000**	**60.000**	**MHz**
			Sch__typ		9.240		
			Sch__etc	**0.051**	10.247	30.220	
			Sch__3std	7.932	9.256	10.579	
			Lay__typ		7.513		
			Lay__etc	**0.043**	8.062	24.922	
			Lay__3std	6.101	7.473	8.846	

DC (dc): Check temperature performance

Name	Parameter	Description		Min	Typ	Max	Unit
IPTAT @ 0.5V output & 25C	**i1__25**		**Spec**	**1.100**	**1.700**	**2.300**	**uA**
			Sch__typ		2.228		
			Sch__etc	1.938	2.221	**2.615**	
			Sch__3std	1.407	2.240	**3.073**	
			Lay__typ		2.228		
			Lay__etc	1.938	2.221	**2.615**	
			Lay__3std	1.203	2.231	**3.259**	
IPTAT temperature coefficient @ 0.5V output	**a1**		**Spec**	**2.500**	**5.000**	**7.500**	**nA / K**
			Sch__typ		7.331		
			Sch__etc	6.515	7.422	**8.577**	
			Sch__3std	5.115	7.104	**9.092**	
			Lay__typ		7.331		
			Lay__etc	6.515	7.422	**8.577**	
			Lay__3std	4.749	7.228	**9.707**	
IPTAT temperature coefficient (avg)	**a__avg**		**Spec**	**2.500**	**5.000**	**7.500**	**nA / K**
			Sch__typ		7.308		
			Sch__etc	6.505	7.405	**8.552**	
			Sch__3std	5.094	7.083	**9.072**	
			Lay__typ		7.308		
			Lay__etc	6.505	7.405	**8.552**	
			Lay__3std	4.749	7.219	**9.689**	
VCTAT @ 25C	**v__ctat__25**		**Spec**	**650.000**	**700.000**	**750.000**	**mV**
			Sch__typ		707.004		
			Sch__etc	705.853	707.002	708.227	
			Sch__3std	686.377	707.450	728.523	
			Lay__typ		707.004		
			Lay__etc	705.853	707.002	708.227	
			Lay__3std	681.281	706.490	731.699	
VCTAT temperature coefficient	**a__ctat**		**Spec**	**-2.000**	**-1.800**	**-1.600**	**mV / K**
			Sch__typ		-1.799		
			Sch__etc	-1.808	-1.796	-1.781	
			Sch__3std	-1.861	-1.804	-1.747	
			Lay__typ		-1.799		
			Lay__etc	-1.808	-1.794	-1.781	
			Lay__3std	-1.869	-1.799	-1.730	
IPTAT error @ 0.5V output	**i1__err__max**		**Spec**	**-30.000**	**0.000**	**30.000**	**nA**
			Sch__typ		8.079		
			Sch__etc	4.222	7.733	24.897	
			Sch__3std	**-62.359**	21.381	**105.122**	
			Lay__typ		8.079		
			Lay__etc	4.222	7.735	**43.486**	
			Lay__3std	**-95.579**	20.118	**135.815**	
IPTAT error @ 0.5V output	**i1__err__min**		**Spec**	**-30.000**	**0.000**	**30.000**	**nA**
			Sch__typ		**-30.769**		
			Sch__etc	**-64.695**	**-34.315**	-23.782	
			Sch__3std	**-124.335**	**-40.876**	**42.583**	
			Lay__typ		**-30.764**		
			Lay__etc	**-108.631**	**-35.679**	-23.779	
			Lay__3std	**-139.525**	**-46.732**	**46.061**	
IPTAT error @ 0.8V output	**i2__err__max**		**Spec**	**-30.000**	**0.000**	**30.000**	**nA**
			Sch__typ		8.083		
			Sch__etc	4.227	7.739	24.864	
			Sch__3std	**-67.319**	22.254	**111.827**	
			Lay__typ		8.083		
			Lay__etc	4.226	7.741	**43.455**	
			Lay__3std	**-94.421**	19.963	**134.347**	
IPTAT error @ 0.8V output	**i2__err__min**		**Spec**	**-30.000**	**0.000**	**30.000**	**nA**
			Sch__typ		**-30.792**		
			Sch__etc	**-64.722**	**-34.350**	-23.801	
			Sch__3std	**-121.815**	**-40.676**	**40.463**	
			Lay__typ		**-30.788**		
			Lay__etc	**-108.654**	**-35.704**	-23.798	
			Lay__3std	**-138.673**	**-46.464**	**45.745**	
VCTAT error	**v__ctat__-err__max**		**Spec**	**-9.000**	**0.000**	**9.000**	**mV**
			Sch__typ		0.243		
			Sch__etc	0.074	0.227	0.283	
			Sch__3std	-0.639	0.373	1.386	
			Lay__typ		0.243		
			Lay__etc	0.000	0.203	0.260	
			Lay__3std	-0.905	0.339	1.584	
VCTAT error	**v__ctat__-err__min**		**Spec**	**-9.000**	**0.000**	**9.000**	**mV**
			Sch__typ		-4.407		
			Sch__etc	-5.385	-4.542	-4.196	
			Sch__3std	-8.778	-4.142	0.494	
			Lay__typ		-4.407		
			Lay__etc	-6.638	-4.562	-4.193	

LELO_GR04_BG_BJT:

LELO_GR04_BG_OTA_PMOS:

LELO_GR04_BG_OUTPUT:

LELO_GR04_COMP:

LELO_GR04_OSC_v2: README.md: “8e12614 Tue Apr 28 20:43:27 2026 +0200”

TB_NCM

This testbench is deprecated in favor of the top-level `LELO_GR04` tests.

Transient analysis (tran): Check transient operation

Name	Parameter	Description		Min	Typ	Max	Unit
Active current	**idd__-45**		**Spec**	**10.000**	**40.000**	**70.000**	**uA**
			Sch__typ		17.126		
			Sch__etc__-notemp	**8.287**	16.891	22.358	
			Sch__3std	**8.979**	17.649	26.319	
			Lay__typ		16.992		
			Lay__etc__-notemp	**7.063**	16.693	22.694	
			Lay__3std	**5.799**	17.211	28.623	
Active current	**idd__125**		**Spec**	**10.000**	**40.000**	**70.000**	**uA**
			Sch__typ		43.457		
			Sch__etc__-notemp	35.249	43.607	54.875	
			Sch__3std	35.648	43.714	51.780	
			Lay__typ		44.480		
			Lay__etc__-notemp	35.903	44.638	56.470	
			Lay__3std	34.119	44.468	54.818	
Leakage current	**iddq__-45**		**Spec**	**0.000**	**50.000**	**100.000**	**nA**
			Sch__typ		0.920		
			Sch__etc__-notemp	0.663	0.784	0.951	
			Sch__3std	0.452	0.823	1.194	
			Lay__typ		1.276		
			Lay__etc__-notemp	0.767	1.558	1.923	
			Lay__3std	0.642	1.564	2.486	
Leakage current	**iddq__125**		**Spec**	**0.000**	**50.000**	**100.000**	**nA**
			Sch__typ		7.084		
			Sch__etc__-notemp	6.275	12.102	34.271	
			Sch__3std	7.003	7.229	7.455	
			Lay__typ		10.187		
			Lay__etc__-notemp	8.696	15.362	38.049	
			Lay__3std	9.793	10.385	10.977	
Oscillation frequency @ -45C	**fosc__-45**		**Spec**	**1.406**	**1.875**	**2.344**	**MHz**
			Sch__typ		2.265		
			Sch__etc__-notemp	**1.114**	2.208	**3.063**	
			Sch__3std	**1.038**	2.306	**3.575**	
			Lay__typ		1.854		
			Lay__etc__-notemp	**0.787**	1.790	**2.462**	
			Lay__3std	**0.681**	1.878	**3.075**	
Oscillation frequency @ 25C	**fosc__25**		**Spec**	**2.081**	**2.775**	**3.469**	**MHz**
			Sch__typ		**3.472**		
			Sch__etc__-notemp	2.647	3.463	**4.745**	
			Sch__3std	2.158	**3.489**	**4.819**	
			Lay__typ		2.823		
			Lay__etc__-notemp	2.194	2.817	**3.760**	
			Lay__3std	**1.660**	2.837	**4.014**	
Oscillation frequency @ 125C	**fosc__125**		**Spec**	**3.598**	**4.797**	**5.996**	**MHz**
			Sch__typ		5.951		
			Sch__etc__-notemp	4.561	**6.020**	**8.180**	
			Sch__3std	4.284	5.956	**7.628**	
			Lay__typ		4.715		
			Lay__etc__-notemp	3.691	4.717	**6.232**	
			Lay__3std	**3.224**	4.710	**6.197**	
Temperature error (calibrated @ 25C)	**t__err__max**		**Spec**	**-10.00**	**0.00**	**10.00**	**C**
			Sch__typ		0.14		
			Sch__etc__-notemp	-2.63	1.71	4.82	
			Sch__3std	**-10.15**	5.10	**20.34**	
			Lay__typ		0.27		
			Lay__etc__-notemp	-2.27	0.24	4.85	
			Lay__3std	**-12.95**	4.36	**21.67**	
Temperature error (calibrated @ 25C)	**t__err__min**		**Spec**	**-10.00**	**0.00**	**10.00**	**C**
			Sch__typ		-4.52		
			Sch__etc__-notemp	**-92.04**	-7.82	-3.33	
			Sch__3std	**-24.96**	**-10.20**	4.56	
			Lay__typ		-7.28		
			Lay__etc__-notemp	**-125.93**	**-11.09**	-5.43	
			Lay__3std	**-38.32**	**-14.81**	-8.71	