LELO_GR02_SKY130A

Who

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Why

Creating this module is part of the Analog Integrated Circuits course at NTNU. The goal is to create a basic temperature sensor and get it to tape out in the TinyTapeout project. Along the way we will learn about the analog design and layout required and gain practical experience working with the tools and understanding the design workflow.

How

This module was developed through four separate milestones, each building on the results of the previous one. A detailed explanation of each circuit can be found under the Schematic section when generating the docs.

Milestone 1 - The Bandgap Circuit

The first step of the project involves designing a bandgap reference circuit. The bandgap is a component used for temperature sensing and/or voltage references in integrated circuits. This circuit generates two key outputs:

- V_CTAT (Complementary to Absolute Temperature voltage): This voltage decreases linearly as temperature increases.
- I_PTAT (Proportional to Absolute Temperature current): This current increases linearly with temperature.

The combination of V_CTAT and I_PTAT allows the system to produce a temperature-dependent signal with a controlled linear relationship. By feeding these outputs into a subsequent oscillator circuit, the temperature-induced changes in voltage and current modulate the oscillator frequency. This frequency can then be measured using a digital counter to accurately determine the temperature of the system

The bandgap simulation shows the leakage current, active current, I_PTAT, V_CTAT, as well as the I_PTAT error and V_CTAT error over a temperature range from 0°C to 70°C.
Observations from the simulation:

- **I_PTAT:** Decreases linearly with temperature, with an error between 0–0.15%. It varies from 2.43 µA at 0°C to 2.85 µA at 70°C.
- **V_CTAT:** Decreases linearly with temperature, with an error between 0–0.08%. It varies from 0.76 V at 0°C to 0.61 V at 70°C.
- **Active current:** At 25°C, it is below 100 µA, meeting the specification criteria.
- **Leakage current:** At 25°C, it is below 1 nA, meeting the specification criteria.

To simulate the bandgap and view plots::

```
cd sim/BANDGAP/
make typical
```

This will display plots for I_PTAT, V_CTAT, and their errors.

Optional: If you do not wish to see the plots, open tran.py in the BANDGAP folder and set:

```
DO_PLOT = False
```

Milestone 2 - The Oscillator

The I_PTAT and V_CTAT from Milestone 1 are used to control the frequency of the oscillator clock. The change in frequency caused by the linear variation of I_PTAT and V_CTAT is how the temperature is measured. As the temperature changes, it affects I_PTAT and V_CTAT, which in turn changes the oscillator frequency. This frequency is fed into a counter (developed in Milestone 3). The counter value is then used to determine the temperature of the bandgap reference.
Observations from the simulation: The figure above is an illustration of the output of the oscillator circuit during transient simulation.

The simulations were run for temperatures -5, 0, 10, 25, 30, 40, 50, 60, 70 and 75 degrees Celsium. The resulting frequency curve is shown below.

To quantify the nonlinearity of the output frequencies, a regression fit was performed and the deviations from the straight line frequency relative to the full scale was plotted below.

This shows that the error from the straight line is between 0.5% and 2.5%.

The regression model and the r^2 correlation figure for both the typical, extreme test case and Monte Carlo simulations can be found on the results page.

The same page contains the power usage measurements. Average active current is currently slightly out of spec at 104 μA typical, 146 μA maximum. The leakage current is currently 19 nA typically, up to 266 nA maximum, way above the 1 nA specification.

The leakage current can possibly be attribtuted to the floating output node. This may be pulled to gnd to possibly reduce leakage. Further optimisations will be performed later.

To simulate the oscillator alone::

```
cd sim/OSCILLATOR
make typical
cicsim wave output_tran/tran_SchGtKttTtVt.raw
```

In cicsim, select v(osc_temp_1V8) to see the output of the oscillator.
To simulate the whole system::

```
cd sim/LELO_GR02
make typical
```

Milestone 3 - The Measurement

With the oscillator from Milestone 2 and the bandgap from Milestone 1 implemented, the next step is to measure the oscillator frequency. The implemented temperature sensor only oscillates while the PWRUP signal remains high (1.8 V). To count the oscillations per system clock cycle, and thus measure the frequency, a circuit that controlls the PWRUP signal is required. This functionality will be implemented in Verilog.
The Counter (counter.v): First, the clock cycles generated by the oscillator must be counted. To accomplish this, an 8-bit ripple counter is implemented in Verilog. The microarchitecture of the counter is shown above. The counter is parametrized to allow for easy arbitrary widths. It is designed to clamp to the maximum value instead of rolling over. This decision was made to have the sensor indicate overtemperature conditions instead of giving a false sense of security by indicating a low temperature.

The counter receives the oscillation signal from the temperature sensor as its clock input and increments its value by one for each clock cycle. For a given oscillation frequency and PVT (process, voltage, and temperature) variation, the counter will reach a specific number of clock cycles within a defined measurement period.

To reset the counter, a reset signal is applied, which forces the counter value to zero. This reset signal is controlled by the state machine.

You can find the implementation of the counter in `rtl/counter.v` and it's accompanying testbench in `rtl/counter_tb.v`. Use `make sim_counter` in the `rtl` directory to run the automated tests and check out `sim/LELO_GR02/sensor_tb_sim.vcd` in your waveform viewer of choice to see the waveform produced by the testbench.
The Finite State Machine (fsm.v): With the counter implemented as shown above, it is now possible to count the clock cycles from the temperature sensor. To control both the counter and the sensor signal, a finite state machine (FSM) is used.
Module Ports:

Port Type	Name	Description	Connection
Input	`clk`	System clock (from Tiny Tapeout).	External signal
Input	`rst_n`	Active-low reset signal used to reset the entire FSM.	External signal (User)
Input	`start_i`	Starts the temperature measurement.	External signal (User)
Input	`cnt_i`	Counter value from the counter module.	Connected to counter's output.
Output	`pwrup_osc_o`	Power-up signal used to turn on the analog temperature sensor.	Connected to PWRUP port on analog design.
Output	`reset_cnt_o`	Active-high signal that resets the counter.	Connected to counter's reset.
Output	`completed_o`	Flag indicating that the measurement is finished and data is ready.	Use as needed.
Output	`clk_cycles_o`	Number of counted clock cycles.	Use as needed.

State Flow & Behavior: The state machine uses three states:

- **Global Reset:** At any time, pulling rst_n low will asynchronously reset the FSM back to the IDLE state.
- **IDLE:** The FSM rests here by default. It holds the counter in reset (`reset_cnt_o = 1`) and keeps the temperature sensor powered off (`pwrup_osc_o = 0`). It waits here until the user drives the start signal high. After a transistion from CAPTURE, the `clk_cycles_o` contains the last oscialltor count with it's validity indicated by `completed_o` (1 means valid).
- **CNT:** Entered with a high start signal. The counter reset is released (`reset_cnt_o = 0`), and the temperature sensor is powered on (`pwrup_osc_o = 1`). After one clock cycle, it automatically transitions to CAPTURE. The counter counts the osciallations of the temperature sensor.
- **CAPTURE:** The FSM powers down the temperature sensor and propagates the counter value and a `completed_o` signal to the output in the next cycle. After one clock cycle, it automatically transitions back to the IDLE state.

Sensor (sensor.v): The FSM and counter are combined in the sensor module. This module contains a reduced set of the in- and outputs as discussed above as well as an input for the oscillator signal (`osc_i`). The module also features two parameters: - CNT_WIDTH: Sets the width of the counter in bits (default: 8). This parameter also exists in and is linked to the submodules for the counter and fsm. - SYNC_START: This decides if a two flip-flop synchronizer is added in the module to synchronize the `start_i` signal into the digial logic's clock domain (default: 0 (false)). If the synchronizer is added, the start signal is delayed by two clock cycles.

Milestone 4 - The Physical Design

The signal flow in the physical layout is roughly left to right. The layout consists of three main cells with their function explained above: The bandgap, the oscillator, and digital layout.

Rules

The following layout rules were applied to ensure the implementation closely matches the schematic:

- **Power rails:** VDD and VSS must be routed with a large width (2 µm) and then distributed to the components. This prevents current loops and avoids connecting component grounds in series, which could lead to uneven current distribution.
- **Metal layer orientation:** Odd-numbered metal layers should be routed vertically, while even-numbered layers should be routed horizontally. This simplifies the layout process and improves consistency.
- **Common-centroid:** Matched circuits like differential pairs and current mirrors must be implemented using a common-centroid layout to minimize mismatch.
- **Trace length:** Interconnects should be kept as short as possible, as longer traces introduce additional parasitic capacitance.
- **Module placement:** For the operational amplifiers, integrate them with the bandgap and oscillator to make efficient use of space. Other modules should be placed to minimize interconnect length between them.

Bandgap Layout: The bandgap consists of the OTA, pnp-based diodes as well as some extra components in the top-level cell. For all of our cells, except for the diode cell, the magic file was generated using `cicpy` before placing and routing manually in magic.

The `BANDGAP_OPAMP` cell consists of two current mirrors, one differential pair, two power gatings, and a second stage. The parallel transistors of the simple current mirror were placed next to each other, with overlapping bulk nodes. This was done to reduce the occupied space and reduce the mismatch between transistors. The PMOS used for the second stage was placed to the right of the current mirror with overlapping source, as it reduced the occupied area. The differential pair were placed in the middle of the `BANDGAP_OPAMP` cell with their bulk node overlapping. With the symmetrical design, the differential pair sees the same, reducing mismatch between the pair. The PMOS power gatings were placed as close to the rail as possible, while the NMOS power gating transistors were placed left to the NMOS simple current mirror. The transistor pulling down the output of the opamp uses the same transistor as a transistor. For the purpose of symmetrical design, the NMOS transistors were placed on each side of the simple NMOS current mirror. The capacitor and resistor were placed at the bottom of the design, such that symmetry is achieved. Compared to the differential pair, the currents through these capacitors does not need to be matched.

The `BANDGAP_DIODE` cell has 9 diodes, in a 1:8 ratio. This enables them to be placed in a 3x3 layout, with the centre being used for the single diode and the 8 peripheral ones connected together. This ensures a symmetric layout.

The `BANDGAP` cell has the OTA with other components placed to the side. Of these, there are 5 PMOS transistors sharing gate, source and bulk. Since this is two double and one single, they are laid out vertically adjacent to eachother in a ABCBA pattern to ensure symmetry. Powergating transistors are placed close to the power rails and connected to the transistors in between. The resistor and and diode cells are placed in between the powergating transistors, to the side of the PMOS transistors. To avoid the cathode of the diode coupling to VSS through the bulk node, it is placed inside of a deep n-well, which provides electrial isolation from the main p substrate. This allows the usage of a powergating NMOS with the drain connected to the cathode of the diodes, instead of directly connecting the cathode to VSS.

Oscillator Layout: The oscillator layout consists of two main parts: the comparator and the flip-flop making up the bridge to the digital section of the chip.

The comparator, similarly to the bandgap explained above, relies on layout symmetry to achieve highly matching device characteristics for the current mirrors and differential inputs thus reducing the circuit's error due to manufacturing imprecisions. The flip-flop, capacitor and power gating transistors do not require such sophisticated placement, making room for the digital design.

Digital Circuit Layout: The digital circuit layout is done using a librelane flow configured in the `rtl/config.json` file. `rtl/pin_order.cfg` contains the input and output pins and their rough placement. Running the flow creates folder `rtl/runs/RUN_<date>/final` containing the designs' performance metrics in `metrics.csv` and layout in `mag/sensor.mag`. The layout size is constrained using the config file to fit in the available area.

What

What	Cell/Name
Schematic	design/LELO_GR02_SKY130A/LELO_GR02.sch
Schematic	design/LELO_GR02_SKY130A/BANDGAP.sch
Schematic	design/LELO_GR02_SKY130A/BANDGAP_OPAMP.sch
Schematic	design/LELO_GR02_SKY130A/BANDGAP_DIODE.sch
Schematic	design/LELO_GR02_SKY130A/OSCILLATOR.sch
Schematic	design/LELO_GR02_SKY130A/COMPARATOR.sch
RTL	rtl/counter.v
RTL	rtl/fsm.v
RTL	rtl/counter.v
Layout	design/LELO_GR02_SKY130A/LELO_GR02.mag
Layout	design/LELO_GR02_SKY130A/BANDGAP_OPAMP.mag
Layout	design/LELO_GR02_SKY130A/BANDGAP_DIODE.mag
Layout	design/LELO_GR02_SKY130A/BANDGAP.mag
Layout	design/LELO_GR02_SKY130A/OSCILLATOR.mag
Layout	design/LELO_GR02_SKY130A/COMPARATOR.mag
Layout	design/LELO_GR02_SKY130A/SENSOR.mag

Signal interface

Signal	Direction	Domain	Description
VDD_1V8	Input	VDD_1V8	Main supply
OSC_-TEMP_1V8	Output	VDD_1V8	Temperature dependent oscillation frequency
PWRUP_-1V8	Input	VDD_1V8	Power up the circuit
VSS	Input	Ground	Ground reference

Internal signals

Signal	Description
PWRUP_N_1V8	Inverted powerup signal
PWRUP_B_1V8	Buffered powerup signal
I_PTAT	Current proportional to absolute temperature
V_CTAT	Voltage complementary to absolute temperature

Key parameters

Parameter	Min	Typ	Max	Unit
Technology		Skywater 130 nm		
AVDD	1.7	1.8	1.9	V
Temperature	-40	27	125	C

Install

Clone LELO_GR02_SKY130A

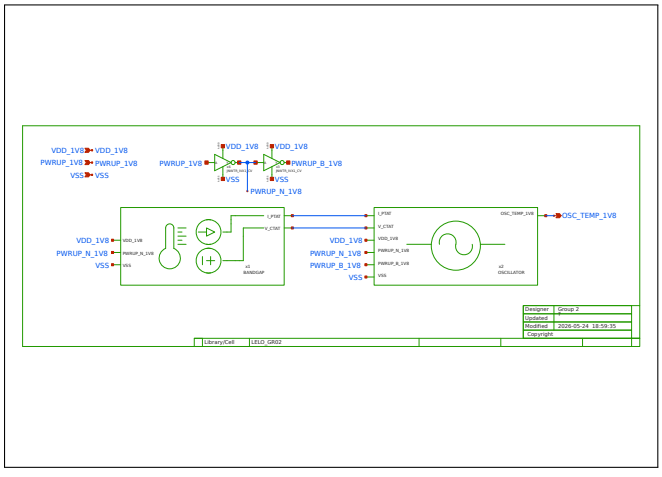
To install, do the following

```
python3 -m pip install cicconf
git clone --recursive https://github.com/analogicus/lelo_gr02_sky130a lelo_gr02_sky130a
cicconf --rundir ./ --config lelo_gr02_sky130a/config.yaml clone --deps
```

Schematics

LELO_GR02_SKY130A

LELO_GR02: This schematic shows the complete system, which consists of a bandgap reference and an oscillator. The bandgap produces a reference voltage and a bias current, which are fed into the oscillator. The oscillator generates a clock signal that is used to drive a counter.



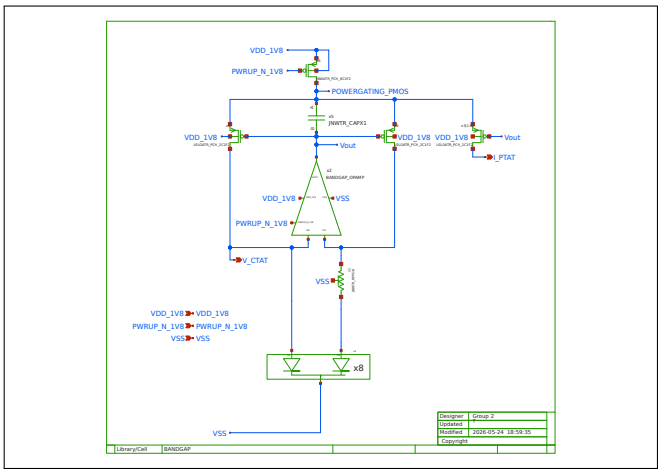
BANDGAP: The schematic depicts a bandgap reference circuit, which provides a temperature-independent voltage reference by combining PTAT and CTAT signals.

The bandgap reference has four inputs and two outputs. The supply voltage VDD_1V8 provides a 1.8 V DC supply to the circuit, while VSS serves as the ground reference.

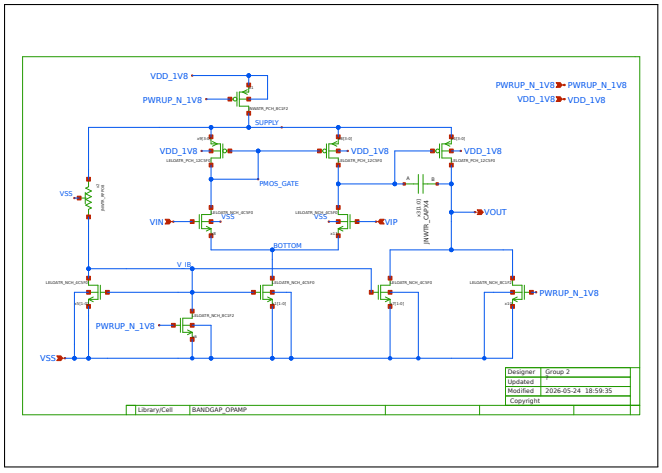
There are two power-up signals; PWRUP_B_1V8, a buffered non-inverted signal used to enable the NMOS transistor for power gating, and PWRUP_N_1V8, an inverted signal used to control the PMOS transistor for power gating. Power gating is implemented to reduce leakage current and overall power consumption when the circuit is not active.

The bandgap circuit generates two outputs: I_PTAT and V_CTAT. The I_PTAT output is a current that is proportional to absolute temperature (PTAT), while V_CTAT is a voltage complementary to absolute temperature (CTAT).

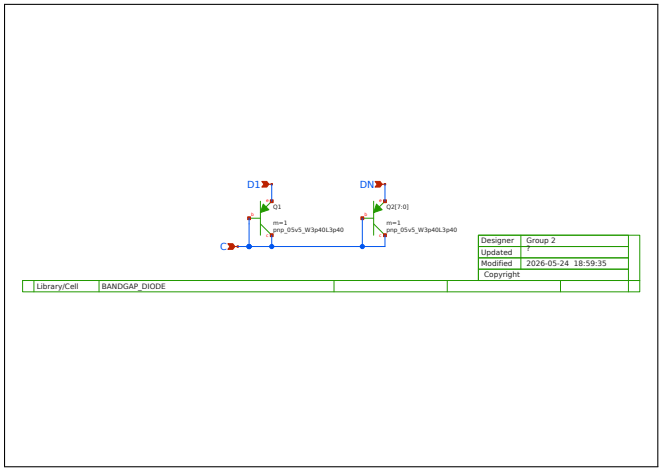
In this system, V_CTAT serves as a voltage reference for the oscillator, while I_PTAT is used to charge the oscillator's capacitor. The capacitor's charging and discharging cycles control the oscillator's frequency, which varies linearly with temperature



BANDGAP_OPAMP: The operational amplifier used within the bandgap circuit is shown in the figure above. It consists of an NMOS differential input pair combined with a PMOS current mirror load to provide amplification. Below the differential stage, a simple NMOS current mirror is used as a current source. A 8 kOhm resistor generates the bias current required to properly drive the op-amp. Power gating for the op-amp is implemented using PMOS transistors located above the circuit. The circuit also consists of a source follower at the output, to increase the opamp gain.



BANDGAP_DIODE: Diodes implemented using NPN BJTs with an area ratio of 1:8.

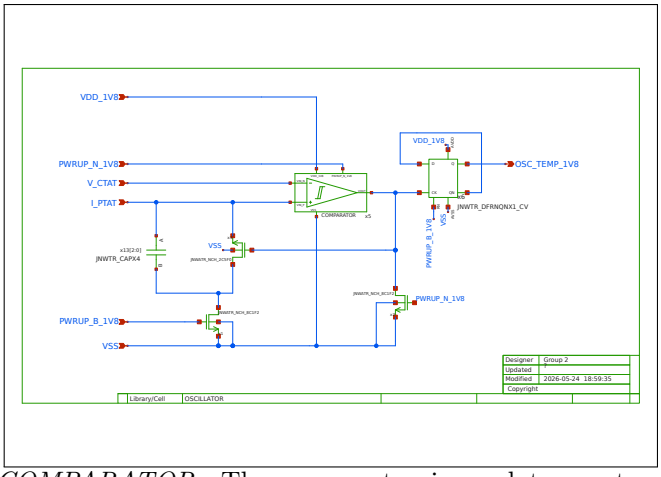


OSCILLATOR: The oscillator is responsible for converting the V_CTAT and I_PTAT produced by the bandgap into a temperature-dependent frequency that can be further processed by digital logic.

To achieve this, a transistor is charged using the I_PTAT current until it reaches the voltage given by V_CTAT. The comparison is performed using an OTA. The output of this OTA drives an NMOS which discharges the capacitor.

Buffers are implemented to introduce a small delay between the NMOS gate and the OTA. This delay ensures that the capacitor has enough time to fully charge or discharge before the gate voltage switches. This prevents incomplete transitions and ensuring stable oscillation.

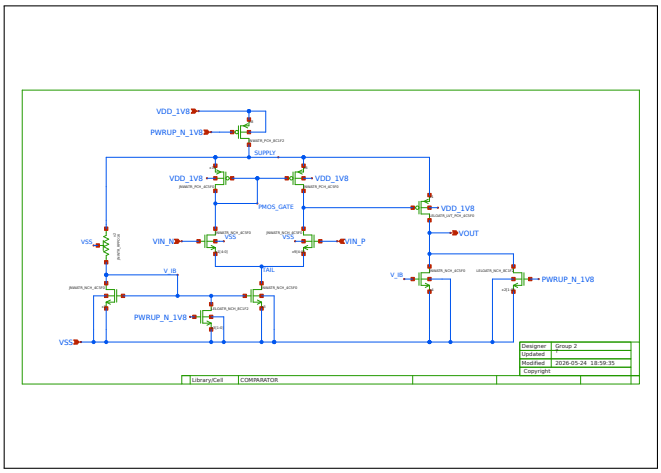
The oscillator serves as the clock signal for a D-FF. The inverted output !Q is fed back to the D input, causing the flip-flop to toggle between 1 and 0 on every clock cycle. The resulting output signal is then used as a counting signal for subsequent digital processing.



COMPARATOR: The comparator is used to create a strong (almost rail-to-rail swing) signal indicating which of the input signals is higher.

At it's center, a differential input pair shares a common source voltage. The current ratio through the two branches of these transistors is proportional to the input voltages. The current mirror converts the differential current into a single-ended voltage with gain. The node labeled TAIL sits right above a current sink that forces a set current through the differential pair, increasing gain and stability. This total current is controlled by the bias voltage V_IB generated by the bottom left current mirror and resistor. The two transistors around the VOUT node make up a second stage amplifier providing additional gain to improve the output swing.

Power gating is used to limit leakage current by turning off the bias voltage node and disconnecting VDD when the comparator is disabled. As a further measure, VOUT is also pulled low when in powersaving mode, avoiding a floating gate on the output.



Simulations

LELO_GR02_SKY130A

LELO_GR02: README.md: “7d6c98f Fri May 1 23:16:56 2026 +0200”

TB_NCM

Transient analysis (tran): Check transient operation

Name	Parameter	Description		Min	Typ	Max	Unit
Oscillation frequency, offset at zero celsius	**freq_-intercept**		**Spec**	**1.000**	**0.000**	**10.000**	**MHz**
			Sch_typ		1.819		
			Sch_etc	1.448	1.860	2.610	
			Sch_3std	**0.073**	1.859	3.645	
Oscillation frequency, increase per kelvin	**freq_slope**		**Spec**	**0.005**	**0.000**	**0.050**	**MHz**
			Sch_typ		0.009		
			Sch_etc	0.006	0.008	0.012	
			Sch_3std	**-0.001**	0.007	0.015	
Oscillation frequency, Pearson correlation coefficient	**freq_rvalue**		**Spec**	**0.950**	**1.000**	**1.050**	
			Sch_typ		1.000		
			Sch_etc	**0.931**	0.957	1.000	
			Sch_3std	**0.106**	**0.850**	**1.594**	
Maximum error from straight line, relative to full scale	**freq_max_-abs_err_-per_fs**		**Spec**	**0.000**	**0.000**	**1.010**	
			Sch_typ		0.000		
			Sch_etc	0.007	0.161	0.319	
			Sch_3std	**-0.348**	0.230	0.808	
Active current at 25 celsius	**i_act_25**		**Spec**	**5.000**	**30.000**	**100.000**	**uA**
			Sch_typ		56.868		
			Sch_etc	44.444	56.864	73.266	
			Sch_3std	50.918	56.958	62.997	
Leakage current at 25 celsius	**i_leak_25**		**Spec**	**0.100**	**1.000**	**1.000**	**nA**
			Sch_typ		0.833		
			Sch_etc	0.717	**5.090**	**35.190**	
			Sch_3std	**-0.031**	**1.496**	**3.022**	

BANDGAP: README.md: “7d6c98f Fri May 1 23:16:56 2026 +0200”

TB_NCM

Transient analysis (tran): Check transient operation

Name	Parameter	Description		Min	Typ	Max	Unit
Current proportial to temperature, offset at zero celsius	**iptat__intercept**		**Spec**	**0.050**	**0.000**	**10.000**	**uA**
			Sch_typ		1.775		
			Sch_etc	2.120	2.433	2.816	
			Sch_3std	0.439	2.578	4.717	
			Lay_typ		2.417		
			Lay_etc	2.120	2.433	2.816	
			Lay_3std	0.073	2.616	5.159	
Current proportial to temperature, increase per kelvin	**iptat__slope**		**Spec**	**0.001**	**0.000**	**0.010**	**uA/K**
			Sch_typ		0.004		
			Sch_etc	0.005	0.006	0.006	
			Sch_3std	0.003	0.005	0.008	
			Lay_typ		0.006		
			Lay_etc	0.005	0.006	0.006	
			Lay_3std	0.001	0.005	0.009	
Current proportial to temperature, Pearson correlation coefficient	**iptat__rvalue**		**Spec**	**0.950**	**1.000**	**1.050**	
			Sch_typ		1.000		
			Sch_etc	1.000	1.000	1.000	
			Sch_3std	1.000	1.000	1.000	
			Lay_typ		1.000		
			Lay_etc	1.000	1.000	1.000	
			Lay_3std	**0.346**	0.962	**1.578**	
Voltage complementary to temperature, offset at zero celsius	**vctat__intercept**		**Spec**	**200.000**	**0.000**	**1200.000**	**mV**
			Sch_typ		726.295		
			Sch_etc	749.855	750.484	751.128	
			Sch_3std	732.593	752.841	773.090	
			Lay_typ		750.436		
			Lay_etc	749.854	750.484	751.128	
			Lay_3std	721.280	751.140	780.999	
Voltage complementary to temperature, increase per kelvin	**vctat__slope**		**Spec**	**-2.000**	**0.000**	**-0.500**	**mV/K**
			Sch_typ		-1.861		
			Sch_etc	-1.772	-1.765	-1.750	
			Sch_3std	-1.780	-1.765	-1.750	
			Lay_typ		-1.766		
			Lay_etc	-1.772	-1.765	-1.750	
			Lay_3std	-1.782	-1.765	-1.748	
Voltage complementary to temperature, Pearson correlation coefficient	**vctat__rvalue**		**Spec**	**-1.050**	**-1.000**	**-0.950**	
			Sch_typ		-1.000		
			Sch_etc	-1.000	-1.000	-1.000	
			Sch_3std	-1.000	-1.000	-1.000	
			Lay_typ		-1.000		
			Lay_etc	-1.000	-1.000	-1.000	
			Lay_3std	-1.000	-1.000	-1.000	
Active current at 25 celsius	**i__act__25**		**Spec**	**5.000**	**30.000**	**100.000**	**uA**
			Sch_typ		42.410		
			Sch_etc	40.888	51.259	66.332	
			Sch_3std	46.879	52.581	58.282	
			Lay_typ		52.168		
			Lay_etc	40.888	51.259	66.332	
			Lay_3std	46.354	52.533	58.711	
Leakage current at 25 celsius	**i__leak__25**		**Spec**	**-0.010**	**1.000**	**1.000**	**nA**
			Sch_typ		0.477		
			Sch_etc	-0.008	0.271	0.594	
			Sch_3std	0.290	0.330	0.370	
			Lay_typ		0.594		
			Lay_etc	0.476	0.616	**9.031**	
			Lay_3std	**-0.923**	0.696	**2.316**	

BANDGAP_OPAMP:
BANDGAP_DIODE:
OSCILLATOR:
COMPARATOR: